N and P Channel ±40V MOSFET

General Description

The JY2504NPM is the N and P Channel logic enhancement mode power field transistors Which can provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used in H-bridge, Inverters and other applications.

FEATURES

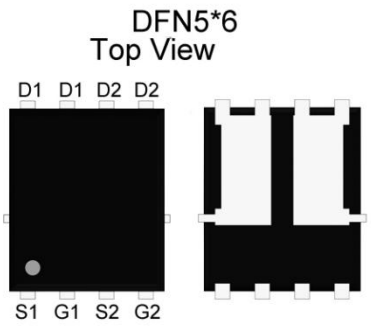
Device	$V_{BR(DSS)}$	$R_{DS(ON)}$ T_J=25° C	Package	I_D MAX T_J=25° C
N-Channel	40V	=12mΩ@V_{GS}=10V	DFN5*6	I_D=30A@V_{GS}=10V
		=15mΩ@V_{GS}=4.5V		
P-Channel	-40V	=28mΩ@V_{GS}=-10V		I_D=-25A@V_{GS}=10V
		=40mΩ@V_{GS}=-4.5V		

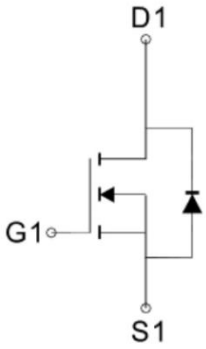
- Low Input Capacitance
- Fast Switching Speed

APPLICATIONS

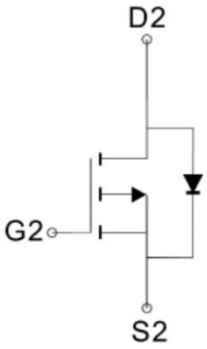
- Power Management
- DC/DC Converter
- DC Motor Control
- LCD TV & Monitor Display Inverter
- CCFL inverter

PIN DESCRIPTION





N-Channel MOSFET



P-Channel MOSFET

N and P Channel ±40V MOSFET

Absolute Maximum Ratings(Ta=25ºC Unless Otherwise Noted)

Parameter		Symbol	N Channel	P Channel	Unit
Drain Source Voltage		V_{DSS}	40	-40	V
Gate Source Voltage		V_{GSS}	±20	±20	
Continuous Drain Current	Ta=25 ºC	I_D	30	-25	A
	Ta=100 ºC		20	-17	
Pulsed Drain Current		I_{DM}	60	-50	
Maximum Power Dissipation	Ta=25 ºC	P_D	36		W
	Ta=70 ºC		25		
Junction and Storage Temperature Range		T_J T_{STG}	-55 to 150		ºC
Thermal Resistance Junction to Ambient		$R_{\theta JA}$	32.5		ºC/W
Thermal Resistance Junction to Case		$R_{\theta JC}$	3.47		ºC/W

Electrical Characteristics(Ta=25ºC Unless Otherwise Noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS},I_D=250uA	N-Ch	1.0		3.0	V
		V_{DS}=V_{GS},I_D=-250uA	P-Ch	-1.0		-3.0	
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±20V	N-Ch			±100	nA
			P-Ch			±100	
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=32V, V_{GS}=0V	N-Ch			1	uA
		V_{DS}=-32V, V_{GS}=0V	P-Ch			-1	
$I_{D(ON)}$	On-State Drain Current	V_{DS}=5V, V_{GS}=10V	N-Ch	60			A
		V_{DS}=-5V, V_{GS}=-10V	P-Ch	-50			
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=10V,I_D=15A	N-Ch		12	15	mΩ
		V_{GS}=-10V,I_D=-10A	P-Ch		28	31	
		V_{GS}=4.5V,I_D=7.0A	N-Ch		15	20	
		V_{GS}=-4.5V,I_D=-5.0A	P-Ch		40	45	
V_{SD}	Diode Forward Voltage	I_S=15A,V_{GS}=0V	N-Ch			1.1	V
		I_S=-10A,V_{GS}=0V	P-Ch			-1.1	

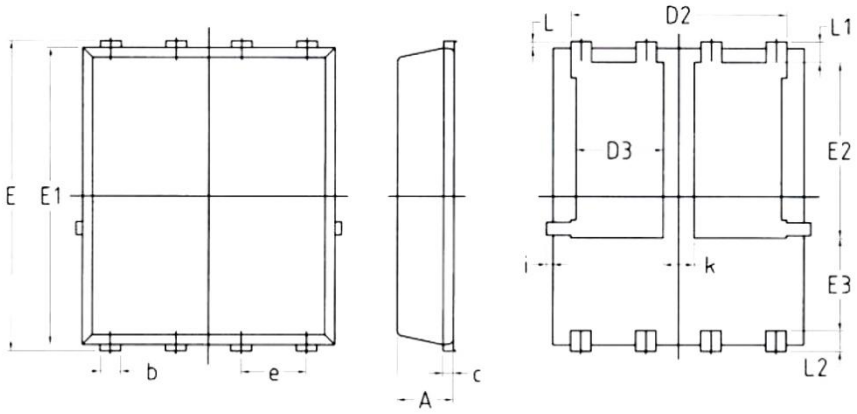
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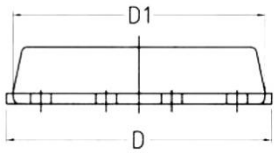
Electrical Characteristics(Ta=25°C Unless Otherwise Noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic							
Qg	Total Gate Charge	N-Channel V_{DS}=20V,V_{GS}=10V, I_D=15A P-Channel V_{DS}=-20V,V_{GS}=-10V,I_D=-10A	N-Ch		18		nC
			P-Ch		16		
Qgs	Gate-Source Charge		N-Ch		3.0		
			P-Ch		2.6		
Qgd	Gate-Drain Charge		N-Ch		2.5		
			P-Ch		2.2		
Ciss	Input Capacitance	N-Channel V_{DS}=20V,V_{GS}=0V, f=1MHz P-Channel V_{DS}=-20V,V_{GS}=0V, f=1MHz	N-Ch		890		pF
			P-Ch		860		
Coss	Output Capacitance		N-Ch		170		
			P-Ch		150		
Crss	Reverse Transfer Capacitance		N-Ch		73		
			P-Ch		69		
$T_{d(on)}$	Turn-On Delay Time	N-Channel V_{DD}=20V,V_{GS}=10V, R_G=3Ω P-Channel V_{DD}=-20V,V_{GS}=-10 V, R_G=3Ω	N-Ch		6.5		ns
			P-Ch		6.0		
T_r	Turn-On Rise Time		N-Ch		13		
			P-Ch		11		
$T_{d(off)}$	Turn-Off Delay Time		N-Ch		19		
			P-Ch		17.5		
T_f	Turn-Off Fall Time		N-Ch		5.6		
			P-Ch		5.0		
T_{rr}	Reverse Recovery Time	I_F=30A, di/dt=100A/us	N-Ch		55		ns
		I_F=-25A, di/dt=100A/us	P-Ch		50		
Q_{rr}	Reverse Recovery Charge	I_F=30A, di/dt=100A/us	N-Ch		24		nC
		I_F=-25A, di/dt=100A/us	P-Ch		24		

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DFN5*6 Package Outline





SYMBOL	COMMON			
	MM		INCH	
	MIN	MAX	MIN	MAX
A	1.03	1.17	0.0406	0.0461
b	0.34	0.48	0.0134	0.0189
c	0.203 BSC		0.0080 BSC	
D	4.80	5.40	0.1890	0.2126
D1	4.80	5	0.1890	0.1969
D2	4.11	4.31	0.1620	0.1700
D3	1.60	1.80	0.0629	0.0708
E	5.95	6.15	0.2343	0.2421
E1	5.65	5.85	0.2224	0.2303
E2	3.30	3.50	0.1300	0.1378
E3	1.70	/	0.0630	/
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.0019	0.0098
L1	0.38	0.50	0.0150	0.0197
L3	0.38	0.50	0.0150	0.0197
i	/	0.18	/	0.0070
k	0.5	0.7	0.0197	0.0276